Electrical characterization of annular Through Silicon Vias for a Reconfigurable Wafer-sized Circuit Board

Mamadou D. Diop[1], Moufid Radji[2], Walder Andre[3], Yves Blaquière[1], Anas A. Hamoui[2], Ricardo Izquierdo[1]

[1] Département d'Informatique, Université du Québec à Montréal
[2]Department of Electrical and Computer Engineering, Mc-Gill University
[3] GR2M, Ecole Polytechnique de Montréal

• Motivation and context

✓Among 3D interconnects, Through Silicon Via (TSV) technology is currently considered one of the most promising concepts that could address the limitations of today's packaging technology.

✓ For the most part, a full filled cylindrical via geometry is used in TSV technology. In the recent years, the annular via geometry has been the focus for industry research institutes and has been demonstrated to have good electrical and thermal performances.

✓This paper presents the electrical characterization of annular TSVs for full wafer application. Results focus on utilization of annular TSVs for a reconfigurable circuit board for rapid system prototyping: the WaferBoard™.

1) Waferboard™: ICs prototype in minutes instead of months

Fig. 1: A 3-D model of the WaferBoard™.

Waferboard™ rapid ICs prototype approach:

1- Open WaferBoard™ cover and place packaged ICs : BGA, QFP…
2- Close the WaferBoard™ cover to press the ICs in place.
3- The WaferBoard™ maps the ICs' contacts and imports the map on your computer.
4- The computer identifies the ICs' contact and specifies their interconnections.
5- WaferBoard™ interconnects the ICs' contacts. The prototype is ready to run.

2) WaferIC™ assembly overview

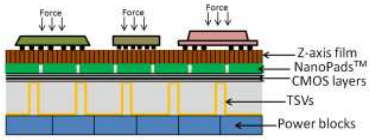

Fig. 2: WaferIC™ assembly schematic.

Annular TSVs are used to feed and configure the WaferIC™ circuitry.

The heart of the Waferboard™ contains a Wafer-sized integrated circuit, the WaferIC™, which is capable of programmably interconnecting ICs' contacts.

• Electrical Results

1) TSV manufacturing

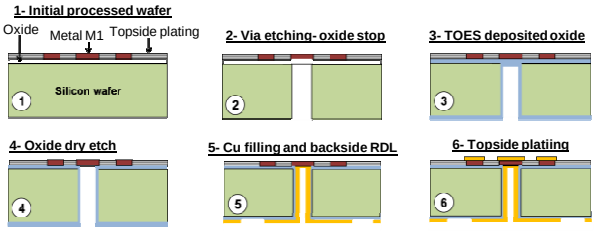

Fig. 3: TSV process flow.

✓ A TSV has 3µm thick annular Cu filling, 110µm diameter and 350µm deep.
✓ 4,864 TSVs are integrated in a 200mm development wafer.

2) Experimental setup

Fig. 4: Development wafer under four probing testing.

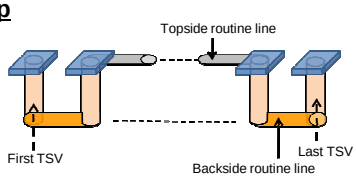

Fig. 5: Schematic of TSV chain for resistance test.

3) Single TSV electrical results

Results	Waferboard™ Annular TSVs	IBM Annular TSVs [1]	Other studies Fully filled TSVs [2]
Single TSV Resistance	10 mΩ	10 mΩ-20 mΩ	20 mΩ-350 Ω
Single TSV Capacitance	0.27 pF	NA	2 fF-1pF

[1] P. S. Andry, et al. "Fabrication and characterization of robust through-silicon vias for silicon-carrier applications," IBM J. RES. & DEV. vol. 52 No. 6 November 2008.
[2] Ioannis Savidis and Eby G. Friedman, "Closed-Form Expressions of 3-D Via Resistance,Inductance, and Capacitance"IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 56, NO. 9, SEPTEMBER 2009.

4) TSV electrical yield at wafer level

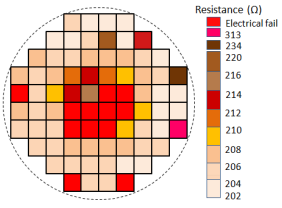

Fig. 6: 76 TSV chains resistance mapping over the wafer.

Dual Beam SEM/FIB images for understanding the TSV electrical failure

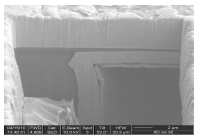

Fig.7: Image of functional annular TSV.

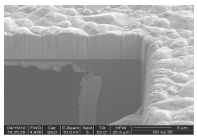

Fig.8: Image of failed annular TSV due poor via filling.

✓ Single TSV resistance is measured by two methods: direct test and 2-TSV chain test.
✓ Electrical wafer yield is obtained by measuring the resistances of all the TSV chains of the wafer.
✓ Individual tests of failed chains allow to find **a yield of 98%.**
✓ Failure of some TSVs is due to poor Cu filling inside the via.

Waferboard™ annular TSVs indicate **low resistance and capacitance** values as well as **high electrical yield at wafer level**

• Conclusion

A TSV technology based on an annular geometry for full wafer applications is described with emphasis on the WaferBoard™, an innovative platform for rapid prototyping of electronic systems. Low resistance and capacitance values at single via level have been obtained. These results, along with the high electrical via yield, show great promise for the full wafer applications. However, optimization of the electroplating process in order to achieve better Cu filling uniformity is necessary.

• Acknowlegment

The authors would like to acknowledge Gestion TechnoCap Inc, DreamWafer® division for their technical support and Intellectual Property, Tower Semiconductor for provision of the Short-Loop wafers and Allvia for TSV processing. Special thanks to Mitacs, FQRNT, NSERC, Precarn and CMC for their financial support.