

Abstract

This paper presents a **programmable interconnection network** for a novel multi-reticle integrated circuit providing a reconfigurable circuit board for rapid system prototyping. This multi-dimensional mesh grid network, called WaferNet™, actively interconnect any pair of pins of integrated circuits deposited on the configurable system board. Two crossbar architectures are implemented and compared, one based on crosspoints and one based on standard cell multiplexers. Implementation results show the feasibility of this proposed cell-based array network that could **interconnect a very large number of nodes**, spread over an area that could fill a whole wafer, using a typical 6-metal 0.18 μm CMOS technology.

Application

- **Programmable Prototyping board** for mainly digital applications
- **Accelerate** by two order of magnitude **prototyping time**, reducing time-to-market and inducing cost-saving
- Huge capacities for routing, great adaptation to user

Context

- **A Reconfigurable Circuit Board** called WaferIC™, which can be larger than a reticle - ultimately a whole wafer - is in development
- **WaferIC™** can have several millions of tiny conducting pads (50μm×50μm) called NanoPads, **over three orders of magnitude denser** than the most complex IC package
- **Any IC package**, with varying spacings and patterns can be **placed anywhere on the surface**
- Package balls will achieve electrical contact with at least two NanoPads

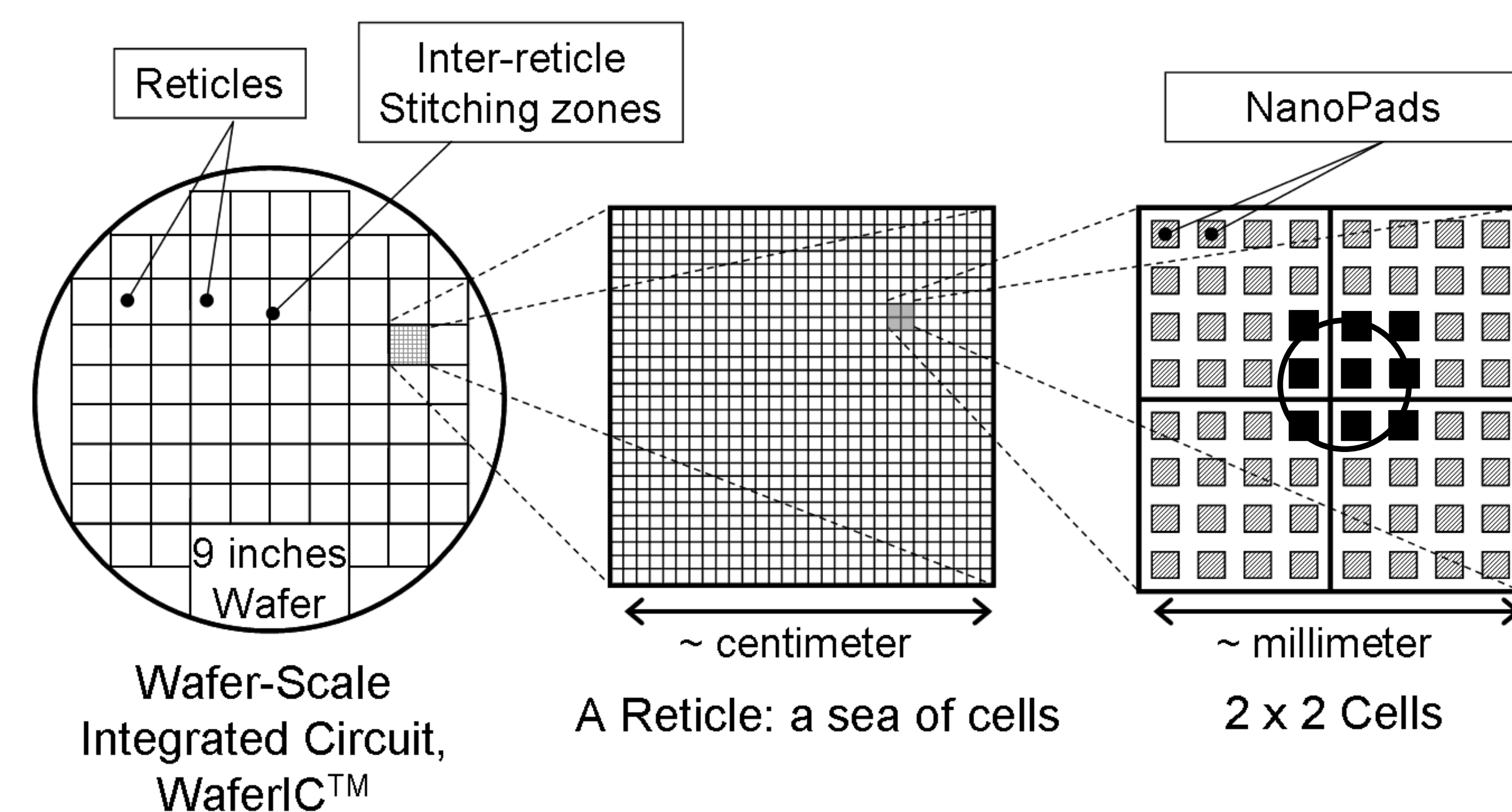


Figure 1: Application global view, at different scales

Architecture

- Sea of identical cells with 16 NanoPads each
- Support up to 2 package balls per cell
- Each cell can be connected to neighbors to redirect signals from/to balls through the NanoPads
- Links in 2 directions (in-out) and 4 dimensions, of length L=1-2-4-8-16-32-64
- **Defect tolerance** is provided by huge number of links
- Great possibilities for routing, **wire density up to 260cm/cm²**

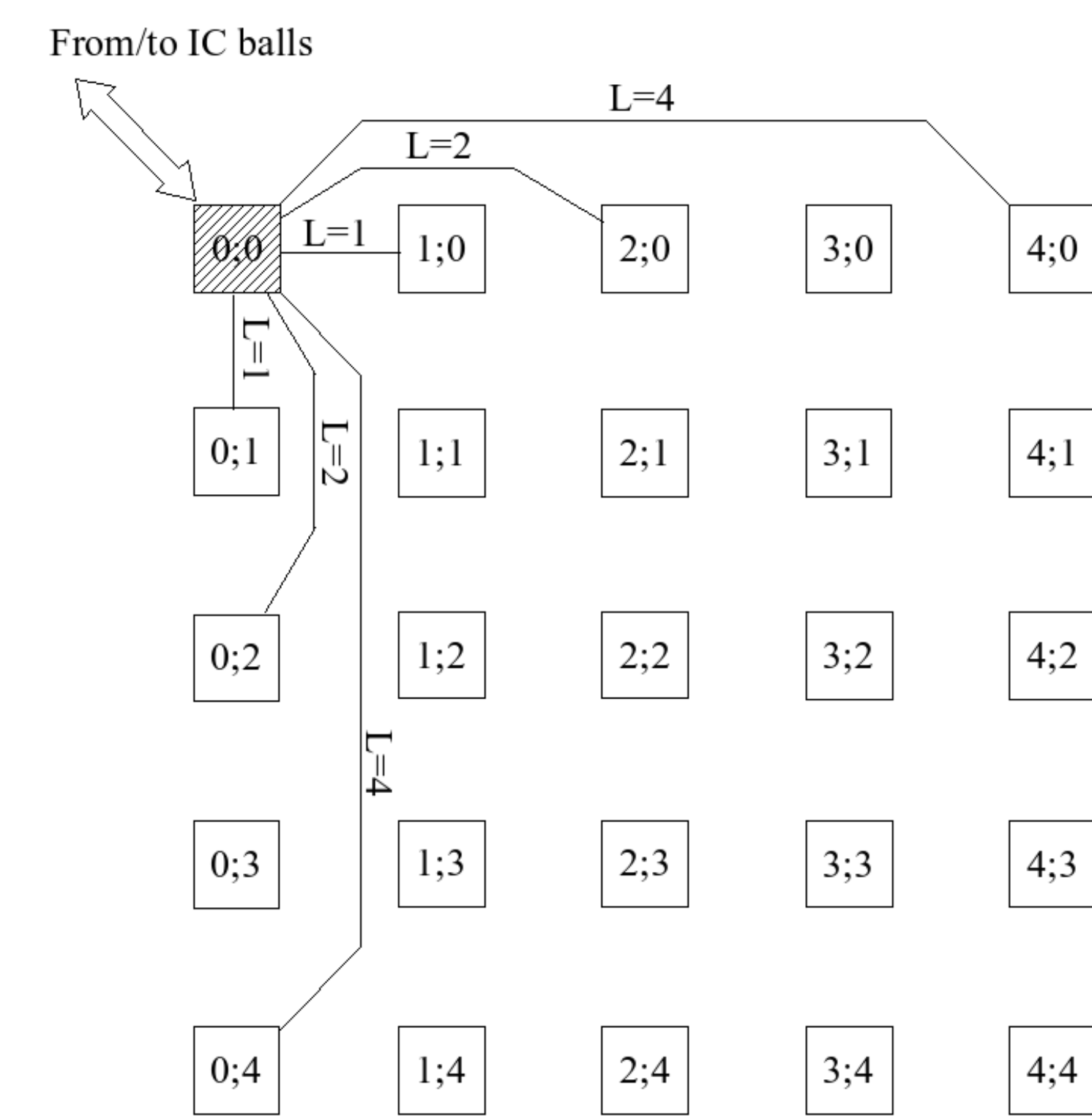


Figure 2: WaferNet schematic view of south and east links for cell [0;0]

Implementation of Two NxM Crossbar Architectures

(1) Tri-State Based Crossbar:

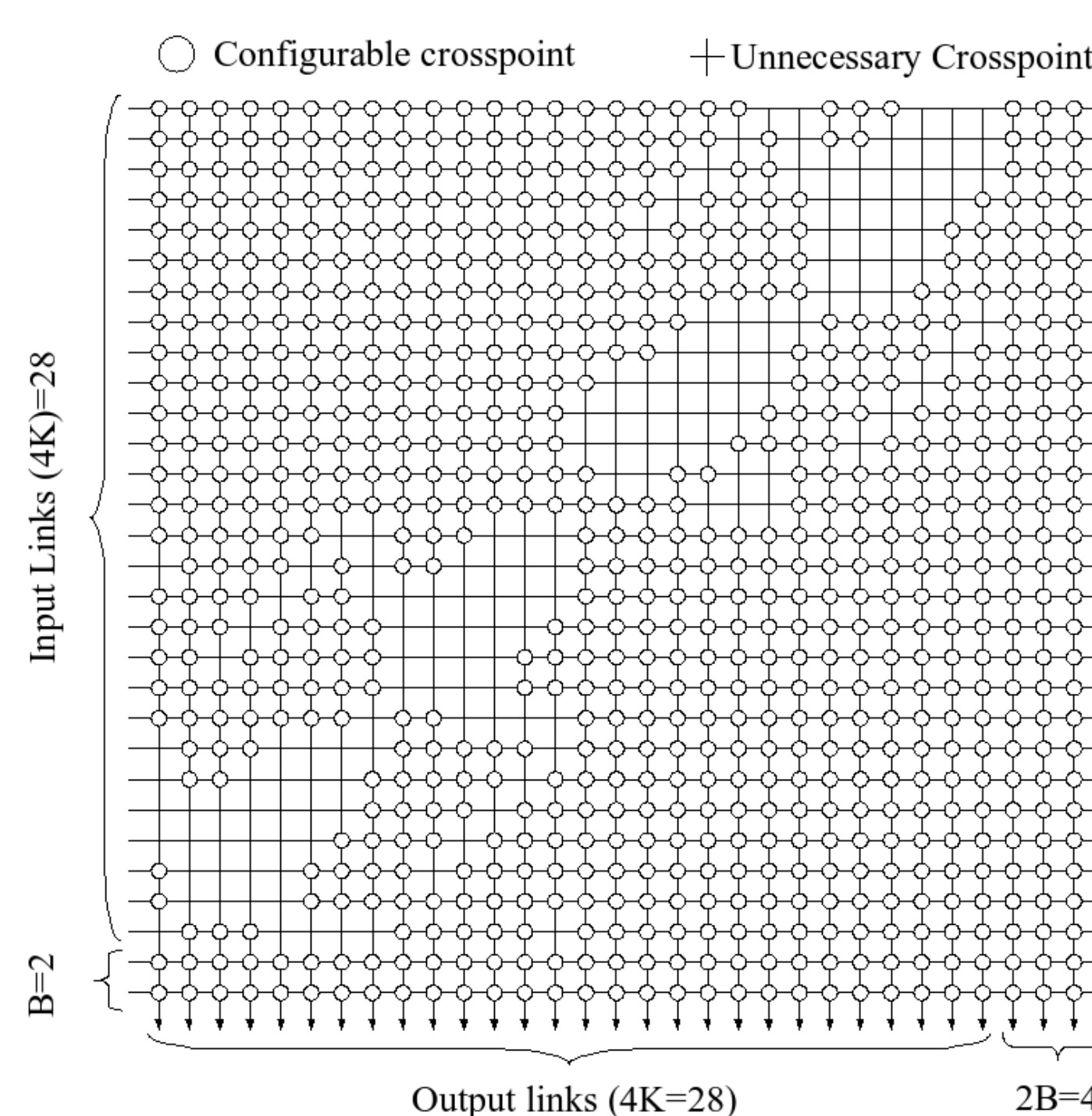


Figure 3: Crossbar schematic view (partial implementation)

(2) Multiplexer-Based Crossbar

- One mux per output
- Area : DFF = $O(\log N)$ and $Mx(N\text{-input Multiplexers})$
- Unidirectionnal
- **No conflicts possible**

- **Very flexible**, provides all possibilities for routing
- Unnecessary crosspoints can be physically pruned (Fig. 3)
- Area = number of crosspoints $O(N^2)$
- Pass transistor: bi-dir, no VTH loss, full custom cell
- Tri-state buffer: standard cell
- May lead to shortcuts

Results Of Four Crossbar Implementations

| Crossbar Type | Total Area (μm ²) | Memory Area (μm ²) | Memory proportion (%) |
|-------------------------|-------------------------------|--------------------------------|-----------------------|
| Full Tri-State Based | 125400 | 54240 | 43.3 |
| Partial Tri-State Based | 91521 | 41764 | 45.6 |
| Full Mux Based | 45050 | 9040 | 20.2 |
| Partial Mux Based | 43538 | 9040 | 20.8 |

"full" is a crossbar with all input to output enabled; "partial" is a crossbar with un-useful links pruned (as in Fig. 3)

- Partial multiplexer-based crossbar occupies 43538 m² i.e. slightly more than 15% of the total area
- Full tri-state based NxM crossbar is three times larger than the partial multiplexer-based crossbar and burst the area budget
- Partial mux-based implementation provides a very low gain compared to full mux-based implementation

Conclusion

This paper has presented a programmable interconnection network for a novel reconfigurable rapid-prototyping system technology, implemented in a large integrated circuit that can scale up to a whole wafer. It provides the ability to:

- Interconnect specified sets of component contacts according to a netlist (user-defined)
- **Defect tolerant**, as required for WaferScale integration, with unidirectional links of length 1, 2, 4, 8, 16, 32 and 64 in each direction and both dimensions.

Implementations with 0.18μm CMOS, 6-metal layer technology:

- Network node area dominated by the crossbar
- Implementation of different crossbar architectures
- Multiplexer-based crossbar is the most efficient in terms of area because the number of configuration memory element is growing in $O(N \log_2 M)$, rather than $O(NxM)$ for crosspoint-based crossbars.

Acknowledgements

The authors would like to thank NSERC and Gestion TechnoCap Inc. for financial support, and CMC Microsystems for providing the design tools and access to technologies.