

A Low-Power, Small-Area Voltage Reference Array for a Wafer-Scale Prototyping Platform

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Abstract— A programmable voltage reference used in an advanced wafer-scale hierarchical voltage regulation circuit is presented. The novel arborescence structure of the voltage regulation system is described and the requirements for the voltage reference derived. The proposed programmable voltage reference is based on beta-multiplier architecture, implemented in 0.18 μm CMOS technology with a very small area of 0.0014 mm^2 . It provides several output voltage references between 1.0 and 2.5 V from an input voltage between 3.0 and 4 V. The overall divergence is less than 10 % from desired output levels, which makes the use of a complete bandgap non-essential for our application. We gave priority to fit in the small allowed area with limited power consumption. The total power consumption of the whole voltage reference module is 386 μW and its static power consumption drops to 0.66 nW when turned off.

I. INTRODUCTION

A novel platform, made of an active reconfigurable waferscale circuit, WaferICTM, has been recently proposed to rapidly prototype digital systems [1]. This platform could be configured to interconnect any integrated circuit (uIC) deposited on its surface by designers. This active surface is composed of several millions of very dense and small conducting pads, called NanoPads. A small array of 4×4 NanoPads is grouped into a Unit-Cell, which are tiled within a reticle (Fig.1). The reticle-image is photo-repeated to build the wafer-scale circuit and uses inter-reticule stitching for connections between reticles. When configured as digital I/O, NanoPads in contact with a uIC ball can be programmably interconnected using a defect tolerant interconnection network.

Each NanoPad can be configured as floating, as a digital input/output, as a power supply or as a ground, according to the type of the uIC ball in contact with. When configured as a power supply or I/O, the NanoPad internal circuit must provide a stable and regulated V_{DD} to its detected uIC load. It has to be programmed to one of the nominal V_{DD} standard levels: 1.0, 1.5, 1.8, 2.0, 2.5 or 3.3 V.

Regulators use a voltage reference that must be internally generated in the Unit-Cell and be configured according to the NanoPad loads requirements. The programmability can be achieved using a DAC coupled with a bandgap reference voltage using PNP parasitic vertical diode but the silicon area

is prohibitive. For example, the circuit proposed by Zhang *et al.* [3] occupies 0.111 mm^2 and is twenty times larger than the available area budget. Others have proposed to use first order delta-sigma modulator to modulate a voltage reference [4], or a variable voltage reference using a feedback control technique to get very low temperature drifting [5], but their areas and power consumptions are too large considering the physical layout constraints of the WaferICTM. These circuits were targeted to ultra-low variation with temperature for precise voltage reference. The NanoPads that supplies power to digital uIC and a 10 % voltage variation is acceptable [2]. This relax requirement allow to build a voltage reference circuit with a much smaller area without the use of a bandgap reference voltage. For our case, the regulator circuit must provide a stable voltage while minimizing temperature deviation.

The millions of NanoPads and the multi-supply voltages needed by different uIC interfaces suggest an hierarchical voltage regulation architecture similar to the one proposed by [2]. The hierarchical wafer-scale voltage regulation circuit and its atypical requirements and constraints on power consumption, silicon area and physical layout are described in section II. Section III presents the programmable voltage reference circuit and its layout. Post-layout simulations and comparisons with existing works are discussed in the same section. They reveal the effectiveness of the approach considering the wafer-scale system environment and constraints. Conclusions are given in the section IV.

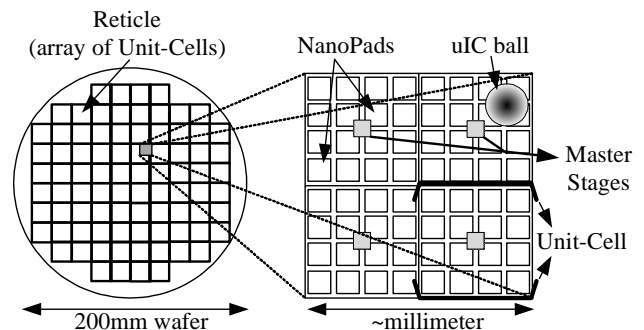


Fig. 1 An active wafer scale circuit with a sea of programmable Unit-Cell that includes 4x4 small conducting pads, called NanoPads.

II. AN ADVANCED WAFER-SCALE HIERARCHICAL VOLTAGE REGULATION ARCHITECTURE

This section briefly presents the architecture to regulate the power supply voltage in the WaferIC™ [1].

A. Wafer-Scale Voltage Regulation Architecture

Switching regulator approaches offer good power efficiency [2] but require large silicon area and off-chip elements. Distributed linear voltage regulators are more amenable into at the wafer-scale prototyping platform that imposes one regulator per NanoPad with very low quiescent current and small silicon area ($< 0.005 \text{ mm}^2$). Hazucha *et al.* proposed a master-slave topology to minimize the silicon area with fast load regulation [2]. The topology in the WaferIC™ Unit-Cell includes one master stage and 16 slave stages (Fig. 1). The 4×4 NanoPads within the same Unit-Cell use the same control signal, V_{SET} (Fig. 2). The master stage main function is to provide a stable control signal, V_{SET} , to these slave stages. This is accomplished using a programmable voltage reference, tracked by an operational transconductance amplifier (OTA), which controls the output of a buffer. This buffer has two properties. The main one is to propagate V_{SET} signal to all slave stages. The second is to shield against all feedback noise that can be generated by the load under regulation. The feedback loop includes a replica of a Fast Load Regulation slave stage that receives the same control signal V_{SET} and returns V_{OUT0} to the OTA input, to insure the tracking of the reference V_{REF} .

The WaferIC power-supply has an arborescence structure (Fig. 3) with a single power-source as the root and the embedded regulator slave stages in NanoPads as the leaves. The WaferIC™ power-structure is organized in blocks, called PowerBlock, which regroup a number of reticles powered-up by discrete regulators providing ground and supply lines of 1.8 V and 3.3 V. A printed circuit board (PCB) filled with regulators supplies all PowerBlocks (the whole wafer) with

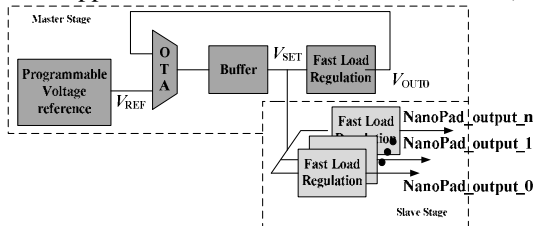


Fig. 2 Hierarchical topology of the embedded regulators in the WaferIC Unit-Cell.

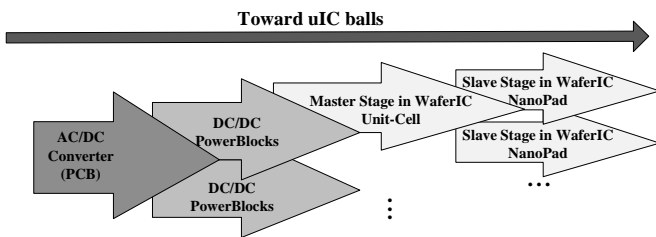


Fig. 3 WaferIC Power-supply arborescence topology.

the needed voltages and grounds. The regulator slave stage embedded in a NanoPad is the closest structure to the deposited uICs and needs to react very quickly to their demanded power.

B. Involved CMOS Design Requirements

Unit-Cells are spread uniformly over the wafer and connect to ground and to other power supplies rails, 1.8 V and 3.3 V, bringing atypical difficulties. The high density of Unit-Cells and NanoPads combined with the power supply arborescence structure make the voltages and ground uneven across the wafer, due to parasitic resistances, process variations, the large number of discrete regulators used in the power-supply chain and random placement of uIC over the surface. These physical and structural constraints make the ground and power grids very noisy. Distributed voltage regulators allow compensating for this matter by being insensitive to DC variations and all frequency noises within the power grids.

To better use of the silicon area the master stage is made external to NanoPads, leaving more area within the slaves for more powerful fast load regulators and larger decoupling capacitances around it to insure their stability. The size of a Unit-Cell is approximately $560 \mu\text{m} \times 560 \mu\text{m}$ with a NanoPad close to $77 \mu\text{m} \times 110 \mu\text{m}$ [1], leaving comparable area for the master stage and other circuits. The area of the programmable voltage reference within the master stage must therefore be very small, less than half of available space (0.00363 mm^2).

The quiescent current of the voltage reference circuit could significantly contribute to the power consumption of the whole waferscale circuit. The master-slave architecture adds a non-negligible advantage of reducing this power consumption by a factor of 16. For example, having one million NanoPads on the wafer with $100 \mu\text{A}$ each would result on a total current of 100 A, which does not make any sense. Therefore, sharing low-power circuitries in the master stage into a Unit-Cell to reduce significantly the power consumption of the whole wafer-scale system.

III. PROGRAMMABLE VOLTAGE REFERENCE

The proposed voltage reference circuit uses a beta-multiplier architecture to provide a current I_{REF} that ideally depends only on transistors parameters (Fig. 4). This current is duplicated into a Programmable Reference Array (PRA) that uses two different voltage divider architectures to achieve targeted values. The voltage selection is made by a series of transistors used as switches (M9 to M13) and control signals (V_{SEL1} to V_{SEL5}).

Transistors M1 to M6 form a cascode current mirror for a good current match between the two branches of the beta-multiplier made of M7, M8 and R[6]. This circuit gives a current I_{REF} in M8 (eq.1) and only depends on transistor parameter β_7 , resistance R and K. The constant β_7 is equal to $K_{\text{PN}} \cdot W_7/L_7$ where K_{PN} is the transconductance parameter of M7. The reference current flowing through transistor M8 is given by equation 1.

$$I_{REF} = \frac{2}{R^2 \cdot \beta_7} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (1)$$

This current is duplicated by transistor M24 in the PRA and fed through one of the five branches by addressing transistors M9-M13 with control signals (V_{SELn}). Having M24 cascode would improve the power-supply rejection (PSR), however stacking two transistors reduces the maximum possible output voltage at V_{REF} below our 2.5 V target. To achieve all targeted voltage references, two different voltage divider techniques are proposed. The first one is used for lower voltage reference. By connecting M14 and M15 gates together and assuming M14 is saturated, M15 is in triode region and their respective drain current (I_{D14} and I_{D15}) are equal to I_{REF} . I_{D14} and I_{D15} can be approximated by equations 2 and 3 where V_{TH} is the threshold voltage, the channel modulation effect is giving by $(1 + \lambda(V_{DS} - V_{DS,sat}))$ and λ_{1-2} is the channel length modulation factor.

$$I_{D14} = \frac{\beta_{14}}{2} (V_{REF1} - V1 - V_{TH})^2 (1 + \lambda_1 V_{TH}) \quad (2)$$

$$I_{D15} = \beta_{15} (V_{REF1} - V_{TH}) V1 - \left(\frac{V1^2}{2}\right) \quad (3)$$

Assuming parameters β_{14} and β_{15} equal, the substitution of equation 3 into 2 gives the expression for V_{REF} (Eq. 4). The reference voltage V_{REF1} is independent on power supply variations according to equations 1 and 4 that are a first degree approximation. The desired levels can be adjusted by varying β_{14} , the sizes of M14 and M15.

$$V_{REF1} = V_{TH0} + 2 \sqrt{\frac{I_{REF}(1 + \lambda_2 V_{TH})}{2\beta_{14}}} - \sqrt{\frac{2I_{REF}}{\beta_{14}(1 + \lambda_2 V_{TH})}} \quad (4)$$

The second voltage divider technique cascades two saturated transistors. With I_{D16} equal to I_{D17} , both currents are derived with equation 5 and 6.

$$I_{D16} = \frac{\beta_{16}}{2} (V_{REF2} - V2 - V_{TH})^2 (1 + \lambda V_{TH}) \quad (5)$$

$$I_{D17} = \frac{\beta_{17}}{2} (V2 - V_{TH})^2 (1 + \lambda V_{TH}) \quad (6)$$

Assuming parameters β_{16} and β_{17} equal, the substitution of equation 6 into 5 gives the expression for V_{REF2} (Eq. 7). This second technique provides higher reference voltage ($>2V_{TH}$) with two small transistors. In opposition the first technique provides smaller reference voltage.

$$V_{REF2} = 2V_{TH} + 2 \sqrt{\frac{2I_{REF}}{\beta_{16}(1 + \lambda V_{TH})}} \quad (7)$$

As stated in the previous section, an important constraint is the quiescent current to be minimized. By scaling correctly transistor M1 to M8 and R, smaller reference current (hundreds of nanos) can be obtained when the voltage reference array is in operation. Transistor M25 is a simple, small area, kill switch function controlled by the signal ON/OFF, which, in suspended mode, disconnects all other transistors by shorting the gate of M1, M3 and M24 to the power supply, cutting any current into the remaining

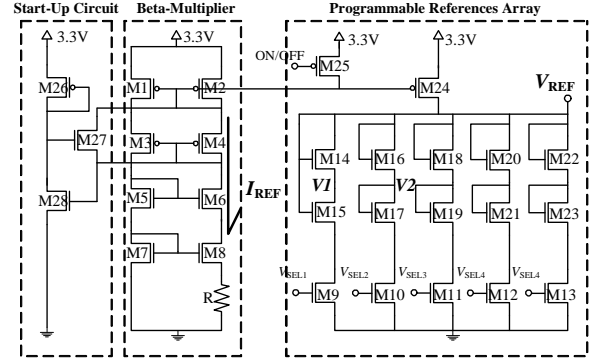


Fig. 4 The proposed programmable voltage reference

structure. Transistors M26 to M28 act as a start-up. At power on, they force transistors M1 to M4 gates to a known voltage for a brief period of time insuring that the cascode current mirror operates correctly.

IV. LAYOUT AND SIMULATION RESULTS

The voltage reference circuit shown in Fig. 4 was optimized to generate nominal digital IC V_{DD} standard levels: 1.0, 1.5, 1.8, 2.0, 2.5 or 3.3 V. The layout in a 0.18 μm CMOS technology within the master stage is shown in Fig. 5. It has a small silicon area of 27 $\mu\text{m} \times 51 \mu\text{m}$ (0.001377 mm^2) including start-up circuitry and the kill switch. Half of this area is used by the beta-multiplier and start-up circuitry (BM-SU) and the other half by the programmable reference array (PRA). Its area is at least one order of magnitude smaller than that proposed by Zhang et al. [3] (Tab. I), which was implemented in 0.35 μm CMOS technology.

Post layout simulations of the programmable voltage reference shows the sensitivity of V_{REF} towards V_{DD} over a power supply sweep from 3.0 to 3.9 at 40 and 100 $^\circ\text{C}$ (Fig. 6). The DC power supply rejection (PSR) varies from 15.1 mV to 84.3 mV per volt, which is less than 4 % deviation from nominal values (not shown on graphs). Temperature deviations are within ~ 2.6 to 9.7 % which is acceptable for CMOS digital circuit ($\sim 10\%$). Fig. 7 shows that the PSR is quite stable for frequency below 1 MHz. Our simulations clearly show that the noise rejection that diminishes at around 10 MHz is due to M1, M2 and M24 gate-source parasitic capacitances. A cascode structure for M24 would contribute to lower this effect, but for reasons explained in previous sections this option could not be retained.

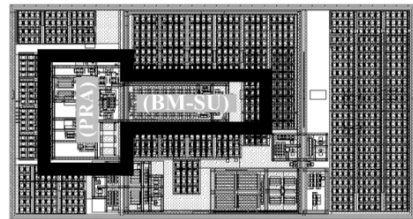


Fig. 5 Layout of the programmable voltage reference array within the master stage

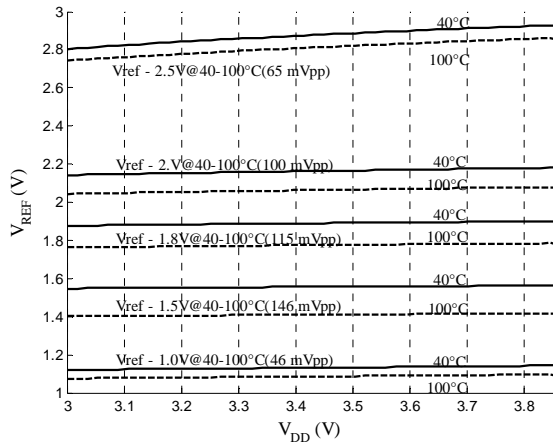


Fig. 6 Reference voltage sensitivity to power supply and temperature variations.

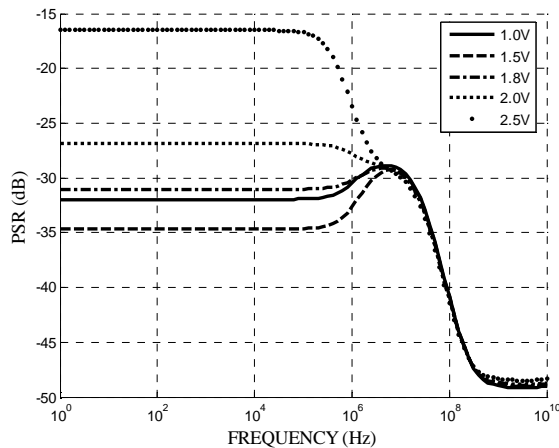


Fig. 7 Power-supply rejection (PSR) of the reference voltage circuit.

Adding a capacitance between the gate and the drain of M24 is another way, which could help cancelling this non-desired effect. At higher frequencies, the circuit act as a low-pass filter, stabilising PSR of all reference to the same level. Comparing the results for PSR of the two different techniques used for voltage divider, shows that the second one (dual transistors in saturation) offers a slightly better power supply noise rejection (~ 5 dB) because both transistors are in saturation region. However the immunity toward power supply for a 2.5 V reference using a 3.3 V power supply is not easily done since the target is very close to V_{DD} . Other properties were extracted from the layout and are summarize in Table I. By scaling down the power consumption and the silicon area, the proposed programmable voltage reference still offers good performances insuring a good noise rejection for all frequencies and a stable voltage reference over V_{DD} fluctuations.

V. CONCLUSION

A unique multi-purpose NanoPad has been introduced in this paper, used in a novel wafer-scale platform for rapid prototyping of electronic systems. This NanoPad can be in

contact with an integrated circuit ball and must be configured as floating, as a digital input/output, as a power supply or as a ground. When configured in supply power mode, it is programmed to one of the nominal V_{DD} standard levels: 1.0, 1.5, 1.8, 2.0, 2.5 or 3.3 V. An existing master-slave voltage regulator architecture was adapted [2] to accommodate the tight and restrictive power and silicon area constraints imposed by the wafer-scale platform. A beta-multiplier based circuit was proposed for a low-power, very small-area programmable voltage reference. The implementation results show an area of 0.0014 mm^2 in a $0.18 \mu\text{m}$ CMOS technology, which is more than one order of magnitude smaller than similar voltage references found in literature. Post layout simulations show mainly an overall $\sim 10\%$ deviation on voltage references for any combination of DC power supply and temperature. The programmable voltage reference includes a kill switch, a necessary feature for a wafer-scale circuit that makes an ultra-low quiescent current of 0.66 nW with a 3.3 V power-supply when in suspend mode.

TABLE I. COMPARISONS WITH PROGRAMMABLE VOLTAGE REFERENCES

Parameters	Zhang et al. [3]	This design *
	Measured	Post-Layout
Technology	$0.35 \mu\text{m}$	$0.18 \mu\text{m}$
Power consumption	ON/ 2.8 mW	ON/ $386 \mu\text{W}$ OFF/ 0.66 nW
Silicone area	0.1137 mm^2	0.001377 mm^2
Power Supply	2.5-5V	3-3.9V
Kill switch	NO	YES
PSR (DC)	$5 \text{ mV}@1 \text{ V}$	$17 \text{ mV}@1 \text{ V}$

*Comparable performances are achieved even without a bandgap topology, with a gain of 100 for silicone area.

ACKNOWLEDGMENT

The authors thank the Natural Sciences and Engineering Research Council of Canada (NSERC), PROMPT Québec, MITACS and Gestion TechnoCap Inc. for their financial support and CMC Microsystems for providing design tools and support.

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