

DreamWafer

Glossary of Terms

Term	Definition
Alignment-insensitive	A system or feature that is not rendered inoperable by small changes in placement or angle of something affixed relative to what it is affixed to.
Alumina, also Aluminum Oxide	A hard ceramic that is both a quite good conductor of heat and an excellent electrical insulator. 96% alumina has a thermal coefficient of expansion that is reasonably well matched to silicon, allowing fairly large regions of the two materials to be attached to each other with temperature changes causing relatively low stress. 96% alumina is commonly used for ceramic 'circuit boards'.
Aluminum Nitride, also AlN	A hard ceramic that is both an excellent conductor of heat and an excellent electrical insulator. Aluminum nitride has a thermal coefficient of expansion that is very well matched to silicon, allowing large regions of the two materials to be attached to each other with temperature changes causing relatively low stress. Aluminum nitride can be used for ceramic 'circuit boards', typically using conductors designed for alumina circuit boards.
Analog	A class of signals where the magnitude of the signal is important, rather than just whether a signal is on or off.
AND	The AND function checks two bits and results in a one only when both bits are one.
Anti-fuse	An insulating link that breaks down to become permanently conductive if a high voltage is applied across it
Areal density	Density per unit area
Array contact	One of a set of contacts roughly equally spaced across a whole surface of a component.
ASIC	An application-specific Integrated Circuit, or an integrated circuit designed and manufactured for a specific application.
ATM, Atmosphere	The typical pressure of the earth's atmosphere, here defined as 100 kiloPascals or 14 Pounds per Square Inch (PSI).
Bare die	A section of a wafer that has been diced (singulated) from the wafer but has not been packaged.
BGA	A ball grid array, or BGA, is a chip package that has an array of solder balls on the bottom, each of which comprises one component contact.
Bump	A very small ball, usually of solder or of gold, affixed to a contact pad.

Term	Definition
Burn-in	A process for increasing the reliability of chips by exercising them for extended periods at full speed, often at elevated voltage or temperature. Chips that survive burn-in testing are unlikely to fail afterward for many years.
Capacitor	Capacitors are small energy storage devices used to keep the voltage from a power supply relatively constant when the current being drawn changes rapidly.
CGA, or Column Grid Array	An array of small columns usually of solder to allow a component to be affixed to a circuit board.
Chalcogenide	A material containing significant amounts of sulfur, selenium or tellurium, which can change from a resistive amorphous phase to a relatively conductive crystalline phase and back through controlled heating and cooling.
CMP	Chemical/Mechanical Planarization, which is a process for planarizing a wafer that basically sands it smooth with a corrosive slurry containing extremely fine abrasive particles.
CMOS	Complementary Metal-Oxide Semiconductor, an energy-efficient type of circuitry that currently dominates the logic-chip industry.
CMOS Wafers	<p>CMOS wafers are wafers of CMOS circuitry, typically made on 8-inch (200 mm) or 12-inch (300 mm) silicon wafers a bit less than a millimeter thick.</p> <p>Specifically in this project, this term is often used to refer to the 200 mm CMOS wafers fabricated using 0.18 micron lithography. These wafers are made with a six-aluminum-metal-layer process, (M1-M6), with stitching between reticles on at least one layer, with the addition of a thick copper 7th metal layer.</p>
CNT	A Carbon NanoTube, which is a small, hollow cylindrical carbon fiber a few nanometers in diameter
Contact pitch, also Contact spacing	The center-to-center distance from one contact to its nearest neighbor contact in a given direction.
Contact Type	The type of contact on a component; see for example BGA, CGA, QFP, Pad and TSOP.
Continuous mesh	A set of links from neighbor-to-neighbor that extends in a given direction for as long as there are neighbors in the given direction to link to.
Critical area	The area of a circuit where small lithographic defects will produce a circuit component that does not function correctly.

Term	Definition
Defect Tolerance	The ability to function correctly in spite of one or more manufacturing defects. Defect tolerance is critical to the WaferBoard because regions with defects cannot simply be thrown away. The JTAG scan and programming chains are defect tolerant, nanopads can be controlled by neighboring cells if their cells are defective, system component contacts will overlap more than one nanopad, and the internal WaferNet™ interconnection network has numerous paths between any set of nanopads.
Dendritic	Having a branched structure.
Development Wafers (Also Post-Processing Development Wafers)	These are wafers made by the wafer fab, but without the device layer and with just one metal layer. The one metal layer has a combination of the M1 and highest CMOS metal patterns. This allows earlier post-processing development and on less-expensive wafers.
Device Layer	The device layer contains the active CMOS circuitry that detects component contacts and supplies programmable power ground and signal connection to them, and also relays signals between component contacts. It is highly defect-tolerant circuitry due to the certainty of having some defects in a whole CMOS wafer.
DRAM	Dynamic Random Access Memory, which is a dense, low-power semiconductor memory that must be rewritten after every time it is read. DRAM is also capacitor-based, and charge gradually leaks from the capacitor; DRAM must therefore also periodically be refreshed.
Fan-out	The number of other entities that a given entity can send to. When used regarding an interconnect network, it refers to the number of entities at the next stage that a given entity at a given stage can send to.
Flexible PCB, or Flex PCB	A printed circuit board where the conductive layers are separated by layers of a flexible plastic.
Flip-chip	A chip that is designed to be affixed circuit-side-down onto a circuit board using solder or conductive adhesive bumps that are typically smaller than 100 micron in diameter on a few-hundred-micron pitch.
FPIC	A Field-Programmable Interconnect Chip, also “FPID” (Field-Programmable Interconnect Device), is a chip that reprogrammably establishes interconnections between any sets of its contacts
FPGA	A Field-Programmable Gate Array is a chip that has contacts, programmable logic cells, and a programmable mesh that interconnects logic cells to contacts and to other logic cells. FPGAs are often used for prototyping, and are increasingly being used for production systems
Higher-dimensional mesh	A mesh that has more logical dimensions than physical dimensions; when used in the context of a planar substrate, it therefore refers to a mesh of at least three dimensions projected onto the two-dimensional substrate.

Term	Definition
H-tree	A branched structure resembling an H, where each arm and leg of the H has a smaller H on its end, and each of those has a still smaller H on each appendage, etc. An H-tree has the same path length to every appendage of the smallest H units, and hence is often used to distribute a signal, such as a clock signal, that is used for synchronization.
Interconnect network	An network that can be configured to establish signal conducting interconnections between sets of elements.
I/O	Something pertaining to Input of a signal or Output of a signal, such as an I/O pin.
JTAG (Joint Test Access Group), also "JTAG port"	A narrow port standardized by the Joint Test Access Group for performing basic tests on a chip, such as checking its scan chain. A JTAG port can also be used for configuring a chip.
M0 (Also 'Backside Metal')	A thick metal layer on the back of the CMOS wafers, currently targeted as five microns (5 μ) of plated copper. M0 is required to keep the solder-ball connection to the TSV from landing right on the TSV, which will not be filled and hence would wick in the solder.
M1	M1 refers to the first CMOS metal layer. This aluminum layer is important to post processing because the TSVs terminate on this layer. M1 connects TSVs through M2-5 to M6 and thence M7 for power and ground distribution in thick layers.
M1 Oxide	M1 Oxide refers to oxide layer below the CMOS M1 layer. This layer is important to post processing because this acts as an etch-stop for etching the TSVs. This oxide is then punched through to connect the TSV to M1.
M2-M6 (Also 'Internal CMOS Metal')	Thin metal layers (aluminum) of little concern to the post processing.
M7	M7 refers to the final CMOS metal layer available on the CMOS wafers. At 3.3 microns thick, this copper layer is thick by CMOS standards, but still thinner than any of the post processing layers. M7 is used for power and ground distribution to the internal CMOS metal layers (the power and ground stripes on M7 are tied into a grid by short connect, and to tie together the post-processed M7 power and ground distribution network. M6 also has signal lines, and also connects Nanopad 'stalks' to the internal CMOS circuitry.
M8	M8 refers to the top layer of the Nanopads, which is a post-processing metal layer around 5 μ thick that protrudes a micron or two above the passivation, rather than being recessed like a typical chip pad. This is an oxidation-resistant pad alloy such as aluminum or nickel-gold, in a layer that is used only for the Nanopad 'caps'.

Term	Definition
MCM (Multi-Chip Module)	Circuit boards made out of layers of ceramic or silicon; MCMs can have much finer wires than a fiberglass circuit board (although still much coarser than on a chip).
Mechanical Housing	The mechanical housing is a sturdy pressure chamber that allows a pressure pouch to apply pressure to hold components onto the WaferIC™ smart surface. The pressure vessel comprises a sturdy lids and a base, both of which also serve as heat sinks, hinged together on one side with a latch on the opposite side.
MEMS (Micro-Electrical-Mechanical-Systems)	Components, usually made through a lithographic process, that contain small moving parts between one micron and one millimeter on a side.
Mesh	A set of links from neighbor-to-neighbor that extends for at least several links in a given direction
Multi-dimensional network	A network where each element has at least one link to at least one neighbor in each of at least two physical or logical dimensions.
Nanopad™	One of a sea of tiny pads that will cover the surface of the wafer. A Nanopad can detect a contact of a component placed on a WaferBoard, and can connect that contact to programmable power or ground or to a configurable internal signal-passing network. The name comes because at the eventual target, for supporting bare dies, of a 30-micon pitch, one billion nanopads fit per square meter.
Nanopad™ Cap	A Nanopad has a 'cap' in M8 that is similar to a chip pad, which is currently targeted as around two microns (2μ) thickness of a typical pad alloy such as nickel-gold. The Nanopad Cap dimensions are targeted at 100μ x 80μ top allow robust contact to components through a z-axis film.
Nanopad™ Stalk	A Nanopad has a 'stalk' in M7 that connects its 'Nanopad Cap' to M6 and thence to the CMOS circuitry. The Nanopad Stalk is currently targeted as a 100μ x 80μ rectangle (possibly with slots through it for power and ground line continuity. With a 140μ Nanopad pitch, this leaves room for metal lines for power and ground between the stalks.
NEMS (Nano-Electrical-Mechanical-Systems)	Components, usually made through a lithographic process, that contain small moving parts between one nanometer and one micron on a side.
Nudge	To move something very slightly, often the smallest amount one can move it.
One-time programmable	Non-reversible programming, such as using fuses or anti-fuses.
OR	The OR function checks two bits and results in a one if either bit is one.
Pad	A flat conductive contact on the surface of a component that connects to circuitry inside the component.

Term	Definition
PCB (Printed Circuit Board)	Refers to both printed circuit boards made by printing the conductive layers in something resembling a traditional printing process, and circuit boards made by depositing layers of copper on insulating sheets and then selectively etching the copper to leave behind the desired patterns.
PCI Express	The SerDes based version of the Peripheral Component Interconnect bus. PCI-Express is used in most computers and workstations for high-performance peripheral cards like network adaptor cards.
Peripheral contact	One of a set of contacts located around the periphery of a component, usually in a ring of pads for a bare die or in a row of wire legs for a packaged component.
Pick-and-place	A machine, or a program for such a machine, that picks components from a dispenser and precisely places them on a substrate such as a circuit board or an MCM.
Point-of-Load Converter, also POL converter	A Point-of-Load converter is a small DC-to-DC voltage converter that is designed to be used close to where the current is drawn. The back side of the WaferIC will be covered with an array of power blocks, each of which contains one or more point-of-load converter and a sea of capacitors.
Power Block, also PowerBlock	A Power Block is a small substrate that contains voltage regulators and capacitors for power-supply integrity. An array of Power Blocks will be flip-chipped onto the back of the wafer (this is the inverse of the normal process into which numerous silicon chips are flip-chipped onto a ceramic substrate). Unless otherwise specified Power Blocks are ceramic to provide a reasonable TCE match to the silicon wafer. Currently the Power Blocks are specified as Aluminum Nitride (AlN) substrates to provide a high thermal conductivity and a reasonable TCE.
Probe card	A circuit board or complex of circuit boards that can make contact with one or more unpackaged components to be tested.
Programmable circuit board	A circuit board that can be electronically programmed to establish interconnections between components.
QFP (Quad Flat Pack)	A flat, rectangular, integrated circuit with its leads projecting from all four sides of the package.
Reprogrammable	Reprogrammable means that allow repeated modifications to the programming.
Reticle, also Reticule, more properly "reticle image"	A reticle image, often just called a reticle, refers to the area of a wafer that is printed as a single exposure through a mask. Normally each reticle contains one or more complete chips that are diced apart and then packaged. However the WaferBoard uses reticles that are stitched together so that the entire wafer is effectively one very large chip.

Term	Definition
Reticle stitching, also inter-reticle-stitching	Reticle stitching is the process of overlapping reticle images slightly in at least some CMOS metal layers to allow dense interconnections between circuits printed in different reticle images.
RF (Radio Frequency)	Circuits or signals that oscillate at speeds comparable to radio signals, with those that oscillate at rates achievable by standard CMOS generally being excluded from the usage. RF is currently considered to start at ten GigaHertz.
Scan chain	A circuit within a chip that tests the chip for defects by sending known values through various functions (typically linking all flip-flops into a long shift-register chain) and reporting the results, usually through a JTAG port.
SerDes	A Serializer/Deserializer circuit that transforms signals from multiple moderate-speed connections into a signal for a single high-speed serial connection, and vice versa.
Signal Contact	A contact that can be used for input or output of a signal, or both, as opposed to a contact for power or ground.
SRAM	Static Random Access Memory, which is a moderate-density, moderate-power memory that can be continuously read and does not need to be refreshed.
Substrate	The wafer on which circuits are built through lithography, or the bare circuit board or ceramic on which a system (such as a power block) is built by affixing components. In the present application 'substrate' generally refers to the wafer in a wafer-based programmable circuit board or the ceramic substrate of the Power Blocks.
System components	Components of a system prototype on a programmable circuit board that would be present if the system being prototyped were to be built on a fixed-function circuit board.
Stuck	An output from a transistor or from a connection or from a pixel that remains the same regardless of the inputs to the transistor or connection or pixel.
TCE	The TCE, or Thermal Coefficient of Expansion, of various materials is a critical factor in this project due to the size of the contiguous region of silicon. To prevent TCE-mismatch induced stress from accumulating over the scale of a wafer, any thick material not TCE-matched to silicon is divided into small regions.
TEOS	Tetra-Ethyl-Ortho-Silicate, or TEOS, is a precursor molecule that easily decomposes in the presence of water into silicon dioxide and ethanol. TEOS is used for depositing silicon dioxide dielectric films at low temperatures.
Trace	A horizontal signal conductive path parallel to the surface of the substrate (as opposed to a vertical 'via').

Term	Definition
TSOP (Thin Small Outline Package)	A thin, rectangular package with leads sticking out the sides of the package. The leads are formed in a J-bend profile, bending underneath and towards the bottom of the package, with gullwing-shaped leads.
TSV	TSVs, or Through-Silicon-Vias, are used to connect the backside metal, M0, to the internal CMOS metal and the CMO circuitry via CMOS M1.
Via	A short vertical conductive path between substrate layers.
Wafer	A thin layer, usually disk shaped and usually sliced from a single crystal of high-purity semiconductor material (chip-grade or circuit-grade). A mechanical-grade 'handle wafer' can be made from the same basic material, but costs less because the material is not as pure and need not be cut from a single nearly-perfect crystal.
WaferBoard™	A novel platform for the Rapid Prototyping of Electronic Systems that uses a wafer-scale interconnect network to programmable power and interconnect component of a system. This lets hardware debug, system integration and software debug to begin immediately, rather than waiting for prototypes to be built on traditional PCBs.
WaferComputing™	Intellectual property that builds on a WaferIC™ base to produce a computing system on a wafer, i.e., processing, memory, and high-resolution display. This includes both embedding processing in the WaferIC™, such as small processors or silicon neurons, and attaching processing to the WaferIC™.
WaferDisplay™	Intellectual property that builds on a WaferIC™ base to produce a computing an extremely-high-resolution display, such as for a heads-up display.
WaferIC™	A Wafer-scale integrated circuit such as the one at the heart of the WaferBoard™.
Wafer Probe card	A probe card that tests (probes) multiple components on a wafer before the wafer is diced into individual components.
Wire-bond	A connection between two contacts made by affixing one end of a tiny bonding wire to each contact, typically through heat or pressure.
XAUI	The Ten-Gigabit Attachment Unit Interface, a SerDes-based interconnect for transferring ten gigabits per second to an external device.
Wafer Probe card	A probe card that tests (probes) multiple components on a wafer before the wafer is diced into individual components.
XOR, exclusive OR	A function that compares two bits and results in a one whenever the two bits differ and a zero wherever the two bits are the same.
Z-axis film (Also ACF)	A thin layer of material that conducts electricity only vertically. A z-axis film is somewhat compliant, allowing chip contacts to be pressed into it to the extent needed to make good electrical connections to the Nanopads on the other side. Also called an 'Anisotropic Conductive Film', or 'ACF'.