

GRD Patent Log

GRD	Description	Author	Pat. No.	Status	Priority Date	Serial No.
	WaferIC – Input/Output Part I					
1	Massively-Parallel Direct Output Processor Array	RN	US 5,801,715	Issued - 1998-09-01	1991-12-06	US 08/323,580
	WaferIC – Defect Tolerance					
2	Efficient Direct Replacement Cell Fault Tolerant Architecture	RN	US 6,154,855	Issued - 2000-11-28	1994-03-22	US 09/376,194
2.1		RN	J 3993634	Issued - 2007-08-03	1994-03-22	JP 7-524267
2.2		RN	K 391805	Issued - 2003-07-03	1994-03-22	K 705245/96
4	Direct Replacement Cell Fault Tolerant Architecture	RN	US 5,748,872	Issued - 1998-05-05	1994-03-22	US 08/618,397
5	Communications Bus For a Parallel Processing System	RN,YB,YS	US 7,546,570 B2	Issued - 2009-06-09	2001-12-20	US 10/324,071
6	Method for Generating Large Scale Signal Paths in a Parallel Processing System	YS,ML,CT	US 6,858,356 B2	Issued - 2005-02-22	2001-12-20	US 10/324,110
7	Fault Tolerant Scan Chain for a Parallel Processing System	YS,ML	US 6,928,606 B2	Issued - 2005-08-09	2001-12-20	US 10/323,896
8	Fault Tolerant Cell Array Architecture	RN	US 7,299,377	Issued - 2007-11-20	1994-03-22	US 10/368,003
9	Semiconductor Wafer on which is Fabricated an Integrated Circuit Including an Array of Discrete Functional Modules	RN	US 6,700,142 B1	Issued - 2004-03-02	2001-12-31	US 10/330,069
10	Fault Tolerant Data Processing System Fabricated on a Monolithic Substrate	RN	US 6,038,682	Issued - 2000-03-14	1994-03-22	US 08/821,672
	WaferIC – Inter-Reticle Stitching					
11	Integrated Circuit Having Lithographic Cell Array Interconnections	RN	US 6,597,362 B1	Issued - 2003-07-22	1991-12-06	US 09/144,695
12	WaveFront Clock Synchronization	RN,DC	US 7,093,150 B1	Issued - 2006-08-15	2001-12-31	US 10/330,068
12.1	WaveFront Clock Synchronization -CONTINUATION	RN,DC	US 7,366,941	Issued - 2008-04-29	2001-12-30	US 11/476,709
	WaferIC – Input/Output Part II					
14	Output and/or Input Coordinated Processing Array	RN	US 6,636,986 B2	Issued - 2003-10-21	1994-03-22	US 10/000,813
14.1	Efficient Direct Replacement Cell Fault Tolerant Architecture	RN	US 6,408,402 B1	Issued - 2002-06-18	1994-03-22	US 09/679,168
14.2	Fault Tolerant Cell Array Architecture - divisional (rename)			Pending	1994-03-22	US 11/872,306
14.3	Fault Tolerant Cell Array Architecture - divisional of 10/368,003			Pending	1994-03-22	US 11/933,705
	WaferIC – Signal Integrity					
15	Methods, Apparatus, and Systems for Reducing Interference on Nearby Conductors	KF,CT,YS, YB,JJL,ZFJ	US 7,609,778 B2	Issued - 2009-10-27	2001-12-20	US 10/022,856
16		YS,YB	US 6,703,868 B2	Issued - 2004-03-09	2001-12-20	US 10/022,852
17		YS,JJL,ZFJ	US 6,897,497 B2	Issued - 2005-05-24	2001-12-20	US 10/023,478
18				Pending	2001-12-20	US 10/022,851
19	Conductive Fabric with Balanced Mutual Interference Amongst Conductors	RN	US 6,951,978 B1	Issued - 2005-10-04	2002-12-30	US 10/739,047
	WaferIC – Mechanical / Packaging					
20	Method for Continuous Linear Production of Integrated Circuits			Pending	1991-12-06	US 10/458,734
21	High-Performance Interconnect Arrangement for an Array of Discrete Functional Modules	RN	US 7,055,123 B1	Issued - 2006-05-30	2001-12-31	US 10/330,231
22	A Connector for Transporting Signals Between Contact Pads on Two Surfaces	RN	US 6,817,869 B1	Issued - 2004-11-16	2001-12-31	US 10/330,232
23	Method & Apparatus Providing Reduced Thermal Expansion Effects on the External Connectivity of a Microelectronic Complex	RN,DC	US 7,279,787	Issued - 2007-10-09	2001-12-31	US 10/330,234
24	Chip and Defect Tolerant Method of Mounting Same to a Substrate	RN	US 6,730,527 B1	Issued - 2004-05-04	2001-12-31	US 10/330,067
25	High Density Architecture for a Microelectronic Complex on a Planar Body	RN	US 7,068,511 B1	Issued - 2006-06-27	2001-12-31	US 10/330,319
26	Flexible Connecting Device for Interfacing with a Wafer	RN,DC	US 6,879,170 B2	Issued - 2005-04-12	2002-06-27	US 10/606,886
27	Connector with Fault Tolerance	RN	US 7,171,584 B1	Issued - 2007-01-30	2002-10-04	US 10/677,333
28	Method & Apparatus for Cooling Microelectronic Complexes including Multiple Discrete Functional Modules	RN	US 6,945,054 B1	Issued - 2005-09-20	2002-10-04	US 10/677,292
	WaferBoard					
30	Reprogrammable Circuit Board with Alignment-Insensitive Support for Multiple Component Contact Types			Pending	2006-12-15	US 11/611,263

28 Patents Issued
5 Patents Pending
33 Total