Reconfigurable Wafer-Scale Circuit Board Steady State Thermal Analysis

Mohammed Bougataya[1,2], Ahmed Lakhsasi[2], Richard Norman, Richard Prytula[3], Yves Blaquière[4] and Yvon Savaria[5]
(1)Université du Québec à Trois-Rivières, (2) Université du Québec en Outaouais, (3) Gestion TechnoCap Inc., (4)Université du Québec à Montréal, (4)École Polytechnique de Montréal,

Abstract:

During the development of a reconfigurable wafer-scale circuit board, the thermal design aspects have proved crucial to its reliable operation. Reducing thermally induced stress and preventing local overheating remain major concerns in maximizing the capabilities of the WaferBoard™ technology. This paper presents thermal analysis of a reliable large WaferBoard™ capable of supporting power-hungry components with various boundary conditions. Several approaches were implemented to achieve a detailed thermal analysis. Device thermo-mechanical behavior is influenced by package geometry, solder balls interconnections, and physical heat source distribution, as well as by the WaferBoard™ design itself.

For this study various thermal boundary conditions are analyzed and thermal profiles along the axes and 3D thermal contours are presented. 3D finite element thermal models are used to predict local thermal peaks on the WaferBoard™ structure. In this way we explore possibilities to minimize the thermal gradient in the critical areas, especially at the solder balls level. In a second step, thermal stress analysis is conducted using the temperature loads calculated by steady state thermal analysis.

Index Terms- Thermal analysis, Heat transfer, *junction temperature,* VLSI, Finite Element.

I- INTRODUCTION

WaferBoard™ is an innovative reconfigurable circuit board for fast system prototyping. This wafer-scale application programmably interconnects integrated circuits and other components at near-intra-chip density. WaferBoard™ supports high pin-count packages of several balls per square millimeter, and provides programmable power and ground as well as signal integrity for programmable chip-to-chip connections.
An innovative approach for designing and implementing a high-density programmable substrate, called WaferBoard™, is described in the paper [1]. This envisioned technology can reduce the cost and development time of complex electronic systems by using a Wafer-Scale Integrated Circuit (WaferIC™) implemented with classical CMOS technologies [2].

Decreasing feature sizes and increasing power and package contact densities are making thermal issues extremely important in the WaferBoard™ design. Thermal analysis is a crucial vehicle for predicting the change in the electrical characteristics or possible stress-induces failure of a WaferBoard™ system. The device requires detailed analysis and optimization of coupling to both a heat-transfer fluid pouch used to apply even pressure, and to an underside heat sink through the WaferBoard™ itself and the supporting structures; i.e. the complete thermal coupling from component to ambient. The accurate and fast evaluation of heat flow patterns becomes an essential step in the overall design verification. The first phase consisted of studying a wide variety of possible thermal scenarios of a WaferBoard™ programmable PCB to have a preliminary idea of its thermo-mechanical behavior.

As processors speeds and circuit densities increase, circuit board power density increases as well and thermal management becomes an increasingly significant part of system design [3]. The final thermal constraint is the silicon junction temperature, which remains a major obstacle for high-end circuit board performance. The miniaturization, the power, packaging, and the computation and communication frequencies of the electronic components all increase the thermal peak loads, and the thermal accumulation is a major limit to circuit and system development. The dynamic behavior of the electronic components is completely different from the static mode. In addition, emerging devices such as micro-electro-mechanical systems (MEMS) require specific packaging techniques, which have to take into account the heat dissipation constraints [4-5].

In this paper, the estimation of thermal peaks and the stress induced on the WaferIC™ (The Wafer-scale circuit at the heat of the WaferBoard™ system) has become the major issue with the increase of the power density and high switching frequency. This investigation uses a thermal heat sources emplacement approach to estimate and predict working temperature of WaferBoard™ structure. In the second step, estimated temperature gradients will be used to calculate stress profiles.

Based on different scenarios, the heat sources placement is introduced. Then finite element analysis is used for

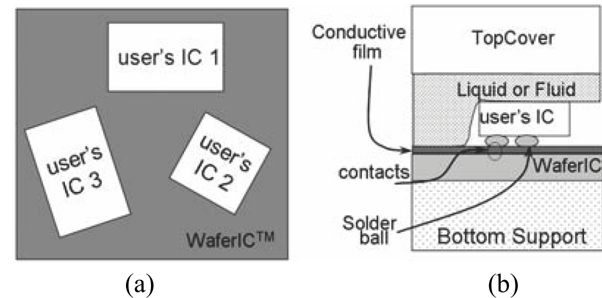
peak temperature prediction during WaferBoard™ operation. In addition, the effect of heat source placement during steady state thermal response is investigated. The model developed can be used for WaferBoard™ accurate rating and appropriate selection of heat sink systems for safe cooling. Therefore, accurate thermal analysis is of crucial importance in the design of the WaferBoard™ to maximize its ability to support high local power densities. However, a major feature of the thermal problem is the need to simulate a very large region of the device and substrate, including the package geometry as well as the WaferIC™ and the supporting and cooling structures. The simultaneous solution of the three-dimensional (3-D) electro-thermal problem is therefore difficult due to the need for very fine meshing of the WaferBoard™ structure at the solder balls and a need for a large simulation region to produce an accurate thermal simulation.

II. THE WAFER-SCALE CIRCUIT BOARD CONCEPT

WaferBoard™ is a reprogrammable circuit board that includes a WaferIC™ in a mechanical chamber with a flat pouch of thermally conductive fluid [1]. This chamber accommodates significant variations in the height of uICs (user ICs) with adjustable uniform downward pressure on all uICs, controlled by a Plunger. The top of the chamber is a large heat sink that can support considerable pressure (up to 10 atmospheres). The backside of WaferIC™ is supported and connected to a mosaic of Printed Circuit Boards (PCB), deposited on but not mechanically bound to a backside PCB, which is itself on a large heat sink TCE-matched to the silicon of the WaferIC™. The WaferBoard™ system has a surrounding PCB that contains permanent affixed components to power the WaferIC™ and uICs, and to provide/get signals to/from WaferIC™ through Flexible PCB connections.

The surface of the WaferIC™ structure consists of a very dense array of very fine (tens of microns) conducting pads, with a compliant contact layer (e.g. Z-axis film or the equivalent, such as deformable gold bumps, or sea of leads) [6] on top. Each pad, called a NanoPad, is connected to an internal wafer-scale interconnect network, WaferNet™ that can be configured to connect any given NanoPad to any others, without conflicting with paths between other such sets of connections. The user's integrated circuit chips can be placed anywhere on the wafer surface (Fig. 1), and the NanoPads are dense enough that each component contact (e.g. solder ball) will touch several NanoPads. Uniform pressure is applied to ensure good contact between the component contacts, and the internal WaferNet™ is then dynamically configured to establish any specified set of connections between the pins/solder balls of those ICs according to a user netlist.

A cell-based architecture is used to obtain a very dense array of NanoPads; the WaferIC™ is a sea of identical cells connected to each other through a huge reconfigurable interconnect network coupled to a dense array of NanoPads. The cell-base architecture dramatically simplifies the design complexity since only one Unit Cell is designed and tiled to form a reticle. WaferIC™ is built from photo-repetition of the cell-reticle; with inter-reticle zones using stitching techniques to ensure connections between reticles [1].



(a) (b)

Figure 1: WaferIC™ top view (a), User ICs on a sea of identical cells, and (b) its application cross-section.

In analyzing heat transfer in the WaferBoard™, it is important to consider the effect of the proximity heat sources. In addition to the normal component junction temperature issue, improper control of the WaferBoard™ temperature can degrade its performance or even induce enough stress to damage the WaferIC™ itself. So the maximum power indicated by the manufacturer of component must be respected at any moment during the operation of the WaferBoard™. Too high a temperature can destroy the crystal lattice of a semiconductor material, so the heat developed inside the material must be evacuated by means of the case and of the heat sink so that the maximum junction temperature T_{jmax} is never exceeded.

III. THERMAL BOUNDARY CONDITIONS

One of the most problematic issues in creating compact thermal models is to use an appropriate set of boundary condition for generating ''data'' with a detailed finite element model representing the thermal envelope of the application. The thermal analysis depends on:

- The cooling option applied,
- The location/vicinity and power of its heat-dissipating neighbors,
- The thermal conductivity of the WaferBoard™ materials: PCB, heat sink, package, substrate and heat spreader.

In this study we use NISA (Numerical Integrated Elements for System Analysis) finite element program to predict inside thermal behavior of WaferBoard™

device. A wide variety of boundary conditions can be applied using NISA [7]. However, the boundary condition on the vertical sides of the simulation region is somewhat problematic. Placing a fixed boundary condition on these surfaces produces a dramatically incorrect result, unless a very large simulation region is used at the expense of very long simulation run times. A more natural boundary condition is a zero flow condition across these tiny surfaces (adiabatic boundary conditions). The remaining boundary conditions to be defined are on the bottom and top surfaces of the WaferBoard™, representing the heat sink interfaces. Because the WaferIC™ is relatively thin and silicon and solder are a good thermally conductors, heat flows mainly towards the bottom, so the boundary conditions in both horizontal directions can be considered adiabatic. The uniform heat removal at the bottom and top is modeled by heat flux exchange coefficient h [W/m^2*K]. The power dissipated in heat sources (components) placed on the WaferIC™ is modeled by heat flux produced into the components. The problem description is presented in figure 2.

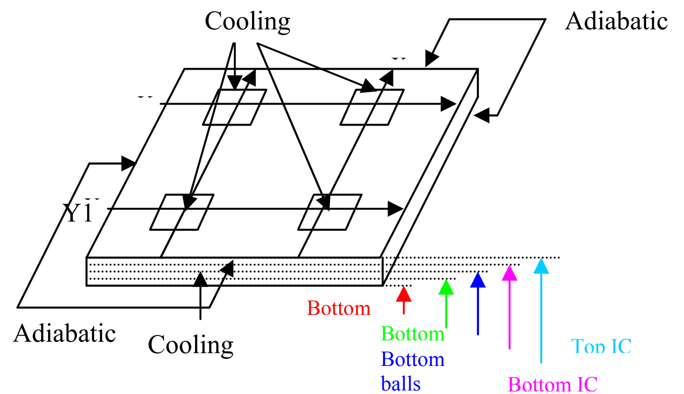


Figure 2: WaferBoard™ inside thermal boundary condition (BC).

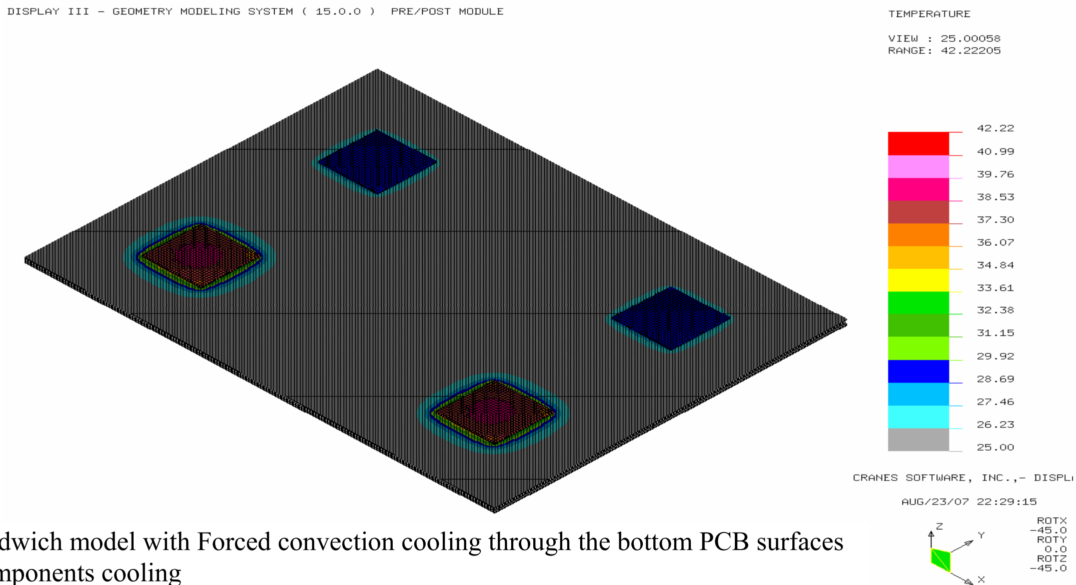


Fig. 3 Sandwich model with Forced convection cooling through the bottom PCB surfaces and on components cooling

IV. HEAT TRANSFER TOOLS USED

NISA is a sophisticated 3-D FEM simulator that has the ability to simulate time-dependent and steady state 3-D nonlinear thermal systems. NISA is an integrated environment, in which a 2-D or 3-D model can be constructed and meshed, boundary conditions set, and the resulting nonlinear set of equations solved. The tool includes a sophisticated DISPLAY4 to aid in building the model and displaying the results.

VI. RESULT AND DISCUSSION

The results give a general idea of the temperatures resulting from the power dissipated by the processor (although this also depends on type of package and heat sink) and the WaferIC™. The biggest heat source is the components and the bulk of the WaferIC™ power is consumed directly underneath. The vertical heat path dominates and is quite independent for each component, so the components can be considered individually. If a 60W Pentium is 40mm square, that 0.0016 square meters. The first impediment to the heat is the pouch material itself; if this is 0.2 mm thick nylon, this is .0002 meters. With nylon conducting 0.3 W/m ^{o}C, this is 2.4W/ ^{o}C so it is expected a 60W Pentium would have a drop of 25°C in the membrane itself *if all 60 Watts were extracted upward*. The top of the pouch contributes very little impedance because the thermal fluid acts as spreader, so the whole area, which 8 times larger, is involved, and the total power of the chips is less than 8 times greater (160W versus 60W).

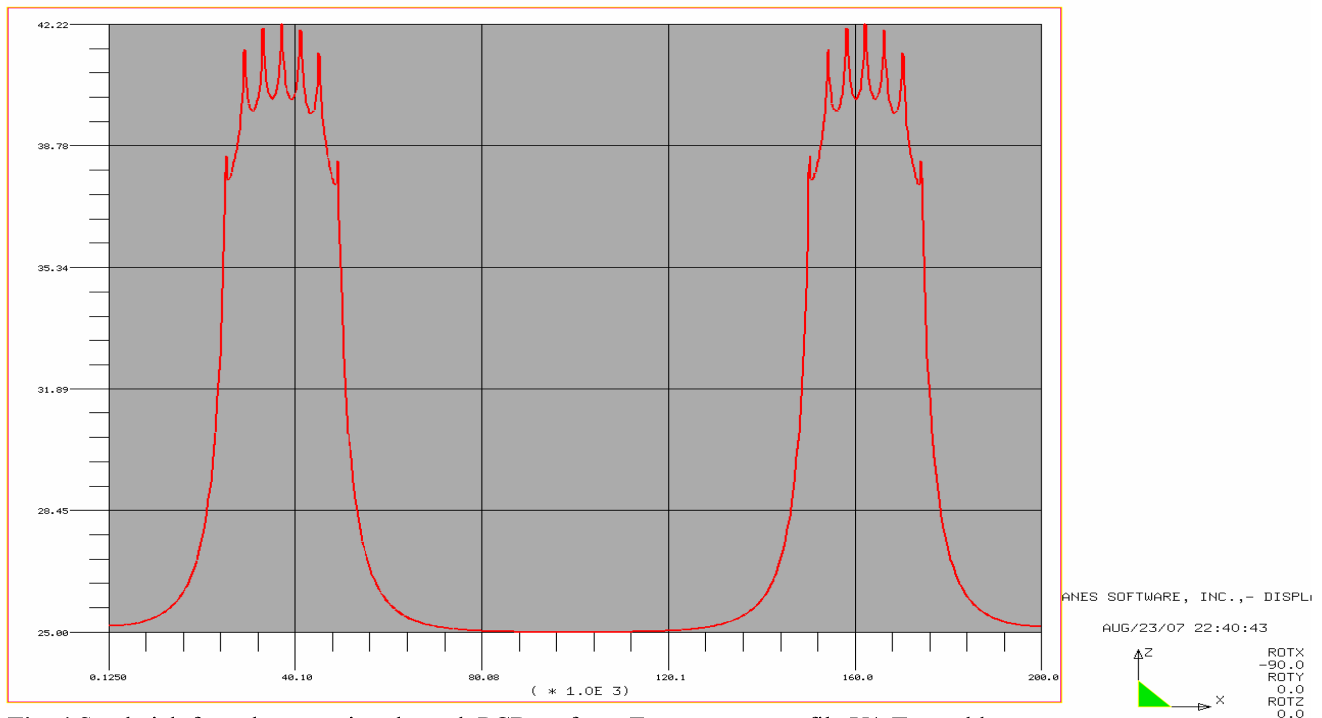


Fig. 4 Sandwich forced convection through PCB surfaces Temperature profile Y1-Top solders balls- WaferIC^{TM}

The heat generated within the wafer has an even easier path to escape, with only 15W under a Pentium-sized chip and no polymer pouch to traverse. The solder balls to the micro-PCBs are very thin, and thus present no significant impedance, and the PCBs can be filled with enough vias to have a thermal conductivity of 20 W/m ^{o}C, so at 3 mm thick, this is about 4W/ ^{o}C for a 40 mm square region. The bottom aluminium heat sink handles only 40W from the whole wafer, and is sitting in an air flow. Thus for the wafer there is only about a 15 ^{o}C rise even under a Pentium due to the WaferIC^{TM}, and heat actually flows from the components through their contacts, through the cooler wafer and through the PCBs. While the direction of the heat flow helps cool the components, the nature of the chip package determines the magnitude by which this reduces the temperature of a given component from that predicted by considering only the pouch. Figure 3 shows thermal iso-contours in the WaferBoard^{TM} structure. Hence, as show in figure 4 and 5 thermal peak occur at Y1-Top solders balls- WaferIC^{TM}.

While the model cannot fully include the lateral heat transfer, the qualitative effects can be analyzed. Given how thin the wafer is, extracting heat laterally through the wafer is of secondary importance. But silicon is an excellent heat conductor, so the wafer acts as a modest heat spreader, reducing the impedance to both heat sinks. To a first order the lateral flow is beneficial, as it reduces both the temperature within the chip and the temperature gradient and induced local stress within the wafer. However lateral flow increases the wafer area that is warmed, increasing wafer warping. The heat flowing laterally is pulled out vertically within millimetres due to the wafer being thin, and so the warping tendency can be overcome with modest applied pressure.

A major feature of WaferBoard^{TM} thermal analysis is the need to simulate a very large region of the device and substrate; in fact the package geometry often needs to be taken into account. Hence, the cost of the thermal management of WaferBoard^{TM} structure depends strongly upon the power density of the individual chips being supported, and moderately on their spatial distribution. These investigations are very useful for the WaferBoard^{TM} project and can help WaferBoard^{TM} design engineers to avoid unexpected pitfalls. These investigations allow an accurate prediction of the temperature distribution in a WaferBoard^{TM} structure and help to keep localized thermal peaks occurring in different layers to a minimum.

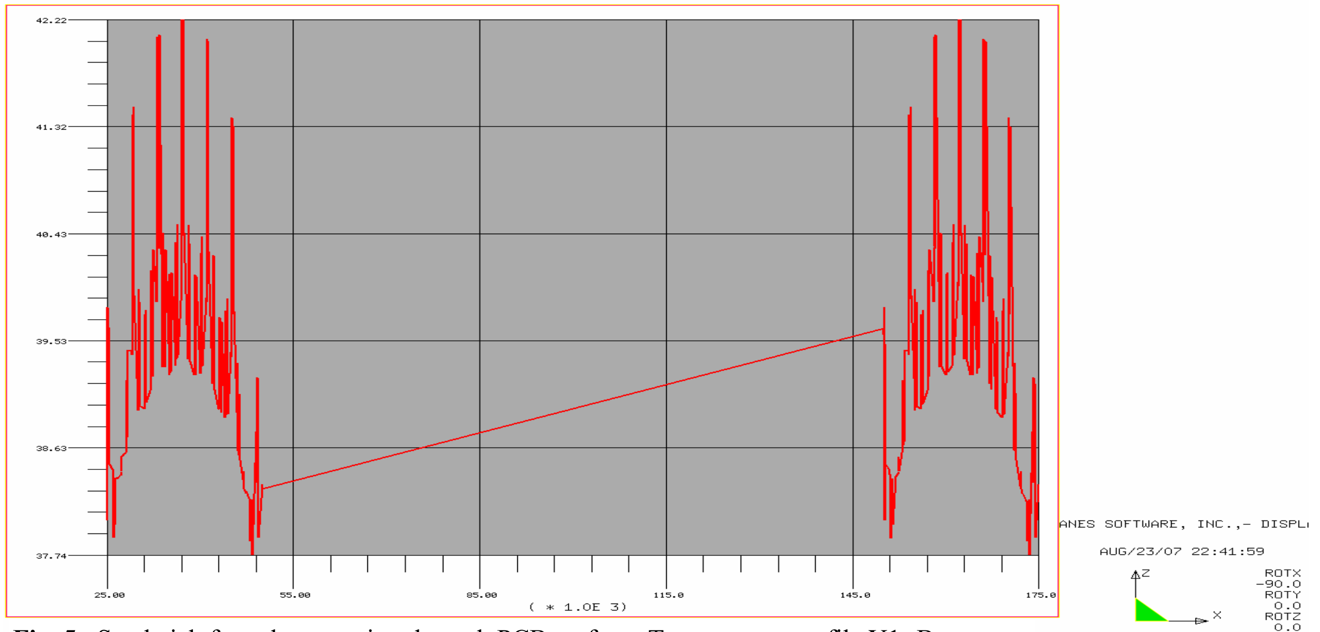


Fig. 5 : Sandwich forced convection through PCB surfaces Temperature profile Y1- Bottom components

VII. CONCLUSION

In this paper, we present reconfigurable wafer-scale circuit board steady state thermal analysis. In this analysis, the temperature of circuit board chip is determined for typical packages. This is an important capability because the cost of the thermal management of electronic systems depends heavily upon the efficiency of the circuit design and because the self-heating of the semiconductor devices can affect the operation of the electronic circuit. Thermal management becomes an increasingly significant part of the design of system and for their correct operation. Moreover, WaferBoard^{TM} thermal analysis is crucial for managing temperature control, spatial thermal gradients, and thermal stress induced. Hence device thermo-mechanical behavior prediction is a major issue for reliable operation, starting from the first step of design of the WaferBoard^{TM} technology.

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