# Thermal Analysis of a Miniature Electronic Power Device Matched to a Silicon Wafer

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*Abstract***— This paper presents the power distribution modules of the WaferBoard™ system. These modules are critical components of these systems. In the proposed configuration, they are TCE (Thermal Coefficient of Expansion) matched to the WaferIC™, a wafer scale device providing a configurable system connectivity. The paper provides results of steady state thermal management investigations that will contribute to its performance characterization. The paper deals with material selection, design, and validation of cooling mechanism to reduce localized hot spots and large thermal gradients. The performance of the proposed power distribution and thermal management strategy was evaluated and tested using a finite element method. Finally, this paper presents the methodology that was used to predict steady state thermal behavior of these critical power devices. It shows the resulting temperature profile when the wafer feeds power to a high performance chip enclosed in a standard package.**

**Index Terms-** thermal evaluation, power device, silicon wafer, AlN substrate.

## I. Introduction

The WaferBoard™ is a rapid prototyping electronic system with an active surface, called a WaferIC™. The WaferIC is a wafer-scale silicon circuit with a dense array of very fine conducting pads on its surface. Each pad is connected to circuits that can detect pins of conventional integrated circuits (ICs) deposited on top of the wafer surface. The wafer can then be configured to create interconnections between components and to power them with proper voltages [1, 2].

The power source for the silicon wafer and the ICs on its top is a key issue. The proximity of the power source to the wafer reduces interconnect length and therefore improves the power supply integrity [3]. The WaferIC cannot be powered with direct connections over to the active surface. The power is supplied from the back of the wafer using through silicon vias (TSV). It is regulated by power devices that embed electronic components such as voltage regulators, capacitors and inductors, surface-mounted on an Aluminum Nitride (AlN) ceramic substrate (Fig. 1). To ensure good electrical contact between ICs, a Z-Axis vertically conductive film and the 350µm WaferIC surface, a strong force is applied on each IC with a uniform pressure. Solid mechanical support, uniformly distributed along the bottom of the silicon wafer is therefore required in order for the fragile mechanical structure to resist such pressure. Several factors impact the mechanical design of the power device (Fig. 1). In addition to the electrical and mechanical concerns, thermal considerations are also critical to the entire WaferBoard and the power device for thermo-mechanical stability [4]. In this paper, a methodology to evaluate and predict a thermal peak of miniature electronic power device matched to a silicon wafer will be presented. The important factors contributing to the device's thermal heating were characterized. The approach reported in this paper can be applied to predict the thermal peak of multilevel structures.

Section II summarizes the constraints on the power device where its major role in the WaferBoard is threefold: electrical, mechanical and thermal. Section III introduces the method used to perform thermal analysis and investigations on the power device, carried out via a 3D thermal model and thermal simulations. Boundary conditions for partially coupled fluid-heat transfer, models and tools are detailed in section IV. Results are analysed and conclusion are presented in section V and VI respectively. It is shown that the power device meets its mechanical and thermal performance requirements.

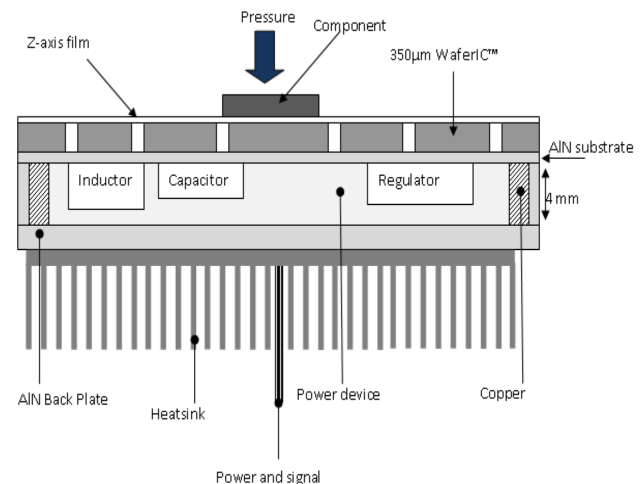


**Figure 1**: The power device at the bottom of the silicon wafer.

## II. POWER DEVICE DESIGN ELEMENTS

Several elements must be taken into account when designing power devices to improve their performance, such as the choice of proper materials, their dimensions and the selection of electronic components that need to be embedded inside.

**Proper materials**: the selection criteria for the power device materials are based on ensuring a good mechanical support to the wafer and on maximizing the thermal conductivity of the power device. Two materials have been investigated for the power device assembly: copper and AlN ceramic. Copper is widely used in the electronic industry for its large thermal conductivity and its strength coefficient, which is close to that of other steels used by mechanical engineers to construct mechanical parts [5]. The second material that was considered is the AlN ceramic. It has a high thermal conductivity and a TCE close to that of silicon. It reduces the expansion mismatch between the power device and the silicon wafer [6, 7], in addition to offering better thermal conductivity.

**Dimensions**: the power device is enclosed between the WaferIC$^{TM}$ (silicon wafer) and the bottom heat-sink (Fig. 1). The thermal conductance of the power device is inversely proportional to the power device height. Thus if the height is reduced, the thermal conductance increases. The height of the power device depends upon the height of the electronic components embedded inside the power device; therefore, the height of the components is an important consideration for improving the power device's thermal conductance. On other hand, the power device area which is a multiple of the size of a printed reticle (2 by 2) is 36×36mm² and it embeds all necessary power electronic components, connectors and heat-sink copper spacers. Finally, these dimensions have a strong influence on the choice of the electronic components.

**Electronic components:** based on an analysis of the system requirements, it was specified that the power device must have the ability to provide up to 100W of electrical power to each region of the WaferIC. The power loss in the power device can increase considerably its internal temperature, which can impact considerably the thermal performance. Therefore, the power device design must take into account the electronic components temperature limit and their size (the smaller the better, in this case).

## III. NEW APPROACH FOR THERMAL INVESTIGATIONS

The electronic components surface mounted in the module reduce the total area available to conduct heat. The materials from which the module is built must conduct heat to the heat sink, but where components and air gaps are present, heat must flow laterally to reach the areas of good thermal conductivity. This greatly exacerbates the challenges associated with thermal management. Overheating in some areas would cause hot spots that not only reduce circuit life, but also induce large thermal stress. A coupled fluid-heat transfer thermal analysis was done. In this case, the thermal behavior depends on the power device geometry and materials, junction structure, and physical heat sources distribution.

The mixed fluid-heat transfer approach for thermal analysis of a thermal path considers large power devices, lateral heat flow through the thin structures, vertical heat flow through the limited thermally conductive area and an estimated convection coefficient of the heat sink. Based on the FEM (Finite Element Method), the approach combines fluid flow and heat transfer analysis to predict working temperature of the wafer scale active surface. Based on this analysis, the effects of power density, position and heat sink characteristics during thermal response can be investigated. The adopted mixed approach can be used for accurate rating of semiconductor devices or heat sink systems when designing large circuits. The proposed approach is an effective design step for high performance power devices.

## IV. A PARTIALLY COUPLED FLUID-HEAT TRANSFER APPROACH

One of the most difficult issues in creating compact thermal models is to use an appropriate set of boundary condition for the finite element model. The accuracy of the calculated thermo-mechanical distributions depends of the boundary conditions that must be selected to reflect the thermal envelope of the application of interest. The thermal analysis depends on the following:

- the applied cooling options;
- the location / power of heat dissipating devices;
- the thermal conductivity of the various materials and components such as: the printed circuit board, heat sink, components package, substrate and heat spreader.

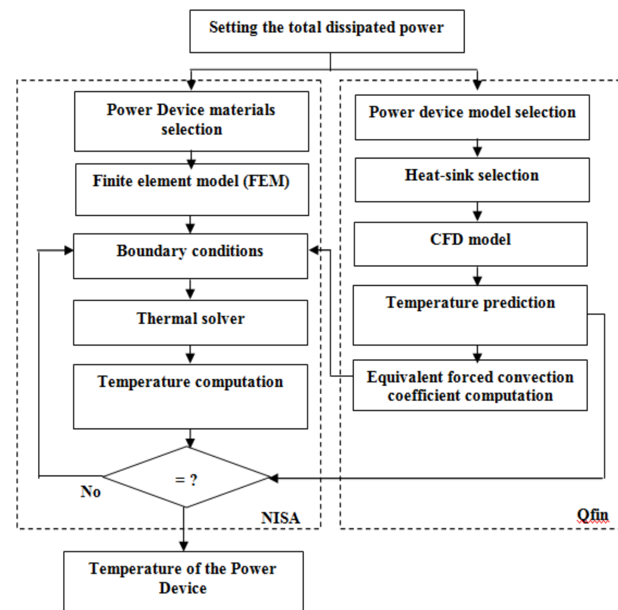


**Figure 2:** Flow chart of mixed fluid-heat transfer approach.

As shown in the flow chart of figure 2, the objective of the approach is to extract the equivalent forced convection coefficient to be applied at the device level. This is achieved in two steps: In the first step, the Qfin software (CFD Computational Fluid Dynamics thermal analysis) is used to determine the heat sink performance. The forced convection coefficient and heat sink configuration are then used to predict detailed power device temperature distribution.

Qfin is used to compute the thermal equivalent forced convection coefficient, which is then used to solve the assembly configuration. The calculation of the heat transfer coefficient is in turn dependant on the type of convection that the assembly is subjected to, as well as the ambient conditions. Hence, an equivalent forced convection coefficient for the whole heat sink model is used as an input to complete the thermal B.C (Boundary Conditions). In a second step of the analysis, NISA (Numerical Integrated element for System Analysis) is used to obtain the same temperature obtained with the equivalent forced convection coefficient computed in step 1.

## V. Examples of Thermal Investigation Results

Two configurations with different floor-plans for the power device are presented. The difference between these configurations is that in the first one, a copper rectangle is fixed to one of the four side of the power device. The role of this copper rectangle is to add mechanical support to the wafer, as well as to increase the thermal conductivity of the power device. For the second configuration a square copper support was added to the center of the power device.

For the thermal investigations, various boundary conditions and approaches (CFD and FEM) were tried to perform a detailed and accurate thermal analysis of the power device feeding nominal power. The convection boundary conditions represented by *h* (forced convection coefficient) applied on the bottom face of the power device were typically between 10-50W/m$^2$ $^o$C). The worst case thermal simulation scenario is a free air convection, which is typically between 3-12 W/m$^2$ $^o$C, when the power loss in the power device is 10 W (when the power device provide 100W to the wafer, the regulator and the other passive components in the power device consume 10W, the specified power loss) and the power dissipated over the silicon wafer is 60 Watts.

The analyses were done assuming forced convection through the bottom. Figure 3 and 5 show the two temperature distributions at the bottom of the power device with a bottom film convection coefficient of 50W/m$^2$$^o$C for the considered power device configurations. Tables 1 and 2 summarize the minimum and maximum temperatures in the power device for different bottom film coefficients, ranging from 10 to 50W/m$^2$$^o$C.

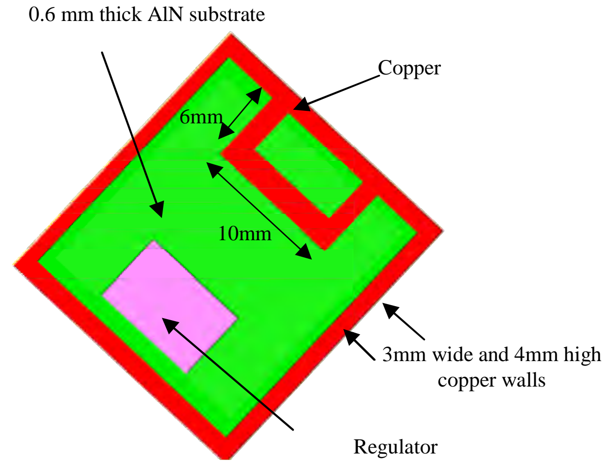


**Figure 2:** First Power device configuration, with copper on the edge

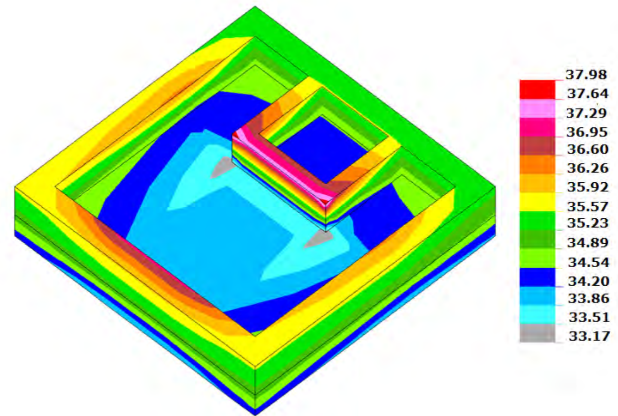


**Figure 3:** Temperature distribution for the first power device configuration

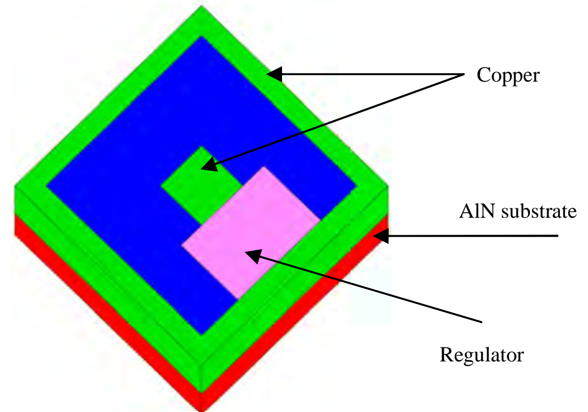


**Figure 4:** Second power device configuration, with copper at the center

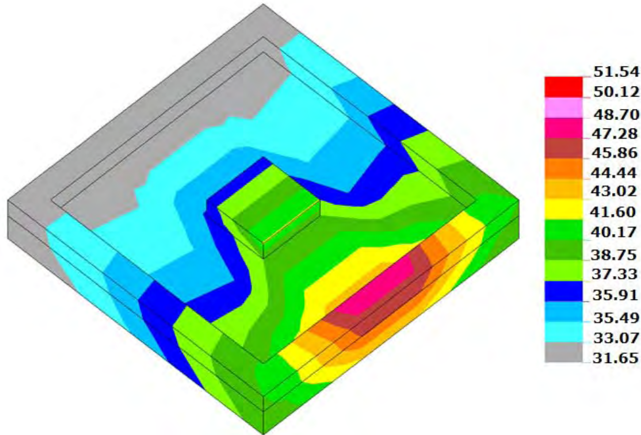


**Figure 5:** Temperature distribution for the second power device configuration.

**Table 1:** Results with different film coefficients

| Bottom film convection coefficient | T min °C | Tmax °C |
|---|---|---|
| 50 W/m² C | 33.17 | 37.98 |
| **40 W/m² C** | 35.34 | 40.16 |
| **30 W/m² C** | 38.97 | 43.80 |
| **20 W/m² C** | 46.24 | 51.09 |
| **10 W/m² C** | 68.09 | 72.95 |

**Table 2:** Results with different film coefficients for the second power device configuration.

| Bottom film coefficient | T min °C | Tmax °C |
|---|---|---|
| 50 W/m² C | 31.65 | 51.54 |
| **40 W/m² C** | 34.02 | 54..53 |
| **30 W/m² C** | 38.14 | 59.34 |
| **20 W/m² C** | 46.68 | 68.71 |
| **10 W/m² C** | 73.09 | 96.09 |

The reported results show that in the first configuration, which is without a central block and with copper on the surface of the power device, the maximal temperature with a bottom film convection coefficient of 50W/m²°C is around 38°C, while the minimal temperature is around 33°C. By contrast, for the second configuration, the maximal temperature increases to around 51.5°C, which is caused by the heat being concentrated behind the regulator, located on the right side of the power device. This reduces the beneficial effect of the central block to reduce the temperatures in the power device. These effects are clearly shown in figures 3 and 5 respectively, with the heat spreading across the power device and the concentration of heat on its right side. A second explanation for these results is the absence of copper on the surface of the power device, in the second configuration, which impedes the desired steady heat spread across the surface of the power device.

## VI. CONCLUSION

In this paper, a methodology to evaluate and predict a steady state thermal behavior of a power device matched to a silicon wafer was presented. The important factors contributing to the device's thermal heating were characterized. The temperature distribution of the power device when supplying power to a high performance chip in a standard package was determined. The modeling approach reported in this study can also be applied to predict the peak thermal stress of high power device matched to a silicon wafer.

Thermal management is a significant consideration when designing power distribution devices and heat transfer structures of the WaferBoard. Moreover, thermal analysis is crucial for managing temperature peaks, spatial thermal gradients, and the thermal stress they can induce. Hence device thermal behavior prediction is a major issue for reliable operation, starting from the first design step of power device technology. Finally, the thermal results presented in this paper permitted evaluating and comparing two configurations of the power device, which is a necessary step towards finalizing the design of the power distribution device.

## ACKNOWLEDGMENTS

The authors thank the Natural Sciences and Engineering Research Council of Canada (NSERC), Le Regroupement Stratégique en Microsystèmes du Québec (ReSMIQ) and Gestion TechnoCap Inc. for their financial support and CMC Microsystems for providing design tools, support and associated technologies. The authors also wish to acknowledge advices provided by Nick Tasker and Jeff Fletcher from Sound Design.

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